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Self-Aligned Single-Crystal Graphene Grains

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The precisely controllable growth of self-aligned single-crystal graphene grains on liquid Cu surface by ambient pressure chemical vapor deposition is reported. Large scale monolayer graphene arrays are modulated by varying growth conditions such as flow rate of carbon source, growth temperature, and growth time. Further, bilayer graphene grains are also controllably prepared under optimized growth conditions. The self-alignment mechanism of graphene is also studied and a growth model is proposed to explain that process involving surface tension of liquid phase. In all, the growth mechanism of graphene arrays is firstly probed and the grown graphene arrays show reasonable mobility and high current density, posing great potential for graphene-based electronics.

1. Introduction

Graphene, a perfect two-dimensional crystal material, has generated enormous interests due to its unique energy band structure and exceptional electronic, mechanical, thermal, and optical properties.[1–3] Monolayer graphene was first obtained through exfoliation of high oriental perpendicular graphite in 2004.[1] Since then, various methods have been developed to prepare graphene, such as epitaxial growth on silicon carbide,[4] reduction of graphene oxide,[5] and chemical vapor deposition (CVD).[6] Among those approaches, CVD is a promising and potentially cost-effective technique to fabricate high-quality and large-scale graphene for industrial development. In the common CVD growth process, transition metals such as Ni, Fe, and Ru[7–9] have been used as catalysts to dissociate carbon sources and to form graphene. Recently, Pt, Ga, and Rh were also employed,[10–12] demonstrating the vast choice of transition metals in preparing high-quality graphene. Our research group has reported that the Cu foil has been used to prepare graphene and then the as-grown few-layer graphene could be employed as an electrode material suitable for low-cost electronics.[13] It is reported that graphene growth on Cu surface follows a self-limited process because of the ultralow carbon solubility in it.[14] Therefore, the Cu foil is of great advantage to high-quality and uniform monolayer graphene growth.[15–19] A typical CVD process of graphene synthesis on Cu can be divided into two stages, nucleation and growth, in which the randomly distributed graphene nuclei would continue to grow and eventually merge into film. Compared with the graphene film composed of numerous grain boundaries,[20] single-crystal graphene domain is more promising candidate for electronic applications and could exhibit more outstanding device performance due to the absence of defects.[21] However, devices based on single graphene domains have been met demanding difficulties in scale-up production because of the small active area and relatively low current. Furthermore, it is still challenging for the prototype device to perfectly integrate into the present manufacturing process. Therefore, well-aligned graphene arrays have the great potential to avoid these problems while still retaining the attractive properties of the individual domain. On the other hand, the single-crystal graphene arrays are conducive to construct high performance device arrays and circuits without complicated processing methods. Based on that, graphene arrays with high quality will find its wide applications in graphene-based electronics for further scale-up production. Thus, realizing the full potential of graphene arrays in realistic electronic systems requires a scalable and controllable synthesis method.

Recently, single-crystal graphene arrays have been prepared by locally controlling nucleation on solid Cu surface with the introduction of pre-patterned solid carbon source, such as poly(methyl methacrylate) (PMMA).[22] Lithographic patterning of the as-grown graphene film was also employed to achieve controllable graphene arrays.[23] However, those methods are time-consuming and high-cost, which limit its wide application in large-scale graphene arrays preparation. Given the complexity of growth parameters related with CVD, processing methods involving catalyst itself need to be proposed. A new method of using liquid Cu as a catalyst to synthesize graphene flakes and uniform film was developed.[18,24] The liquid characteristic of the liquid Cu allows the control of graphene nucleation due to the less grain boundary comparing to solid Cu surface, thus leads to large single-crystal graphene domains. However, at present it is still a great challenge to precisely tailor the distribution of graphene nucleation on Cu surface by CVD and thus the arrangement of grown graphene grains is not well controlled. Meanwhile, the growth model of graphene arrays is not established and the related mechanism is also not investigated.

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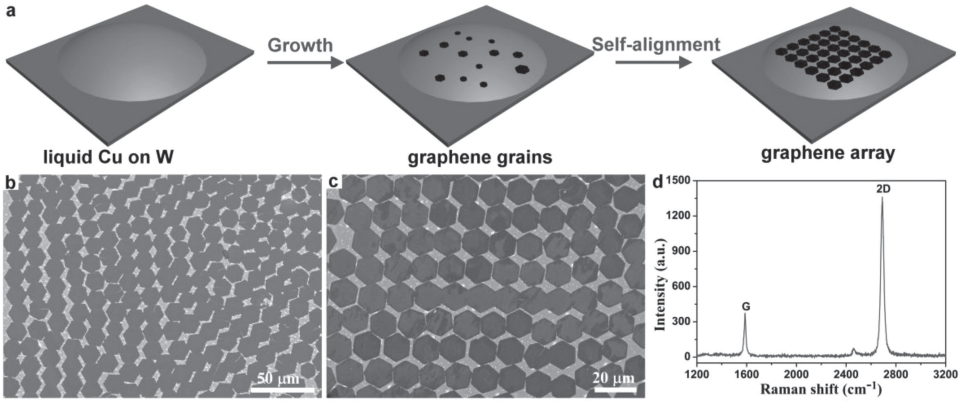

Figure 1. Growth of self-aligned graphene arrays on liquid Cu. a) Schematic illustration showing growth of self-aligned graphene arrays by methane-CVD method. b, c) SEM images of single-crystal graphene arrays at low and high magnifications, respectively. These hexagonal graphene arrays were grown on liquid Cu using 5 sccm (standard cubic centimeters per minute) CH_4/300 sccm H_2 at 1160 °C for 30 min. d) Raman spectrum of as-grown individual graphene domain, indicating the monolayer characteristics.

Here, we report the use of liquid Cu to precisely control growth of self-aligned hexagonal graphene grains by methane CVD at ambient pressure and then study how the adjacent graphene flakes are arranged into uniform graphene arrays. By controlling the growth parameters, for example, methane (CH_4) flow rate, well-dispersed and single-crystal graphene arrays were prepared. Further, bilayer graphene were also fabricated under optimized growth conditions, demonstrating the high controllability over graphene layer numbers using this method. We systematically studied the effect of carbon flow rate on the size evolution and arrangements of graphene flakes. Then the grown graphene arrays were transferred onto 300 nm SiO_2/Si substrates for further characterization and the experimental results clearly showed high quality and good carrier transport properties. Moreover, the self-aligned growth mechanism was discussed and thus a growth model was established.

2. Results and Discussions

Graphene arrays were synthesized by ambient pressure chemical vapor deposition on liquid Cu surface as schemed in **Figure 1**a. This method involves the formation of liquid Cu phase on tungsten (W) substrate at the growth temperature above Cu melting point (1084 °C). Considering the existence of liquid phase, W foil was chosen as a supporting substrate due to its good wettability for the liquid Cu. When the furnace temperature reached 1160 °C, followed annealing in hydrogen (H_2) gas for 30 min was in process, during which solid Cu foil would become liquid phase and thus the pre-existed grain boundaries would disappear and the liquid Cu surfaces would change into uniformity from a macro-view (Figure S1, Supporting Information). Based on that, liquid Cu provides a much more homogeneous surface by essentially eliminating some active sites related with steps, grain boundary of Cu, resulting in uniform nucleation density compared to using solid Cu foil. During the graphene growth stage, CH_4 was introduced into the reactant chamber as the carbon source and hydrogen as activator of the surface bound carbon.[25] After the introduction of CH_4 and H_2 for a certain time, the hexagonal graphene islands grew from nuclei and laterally expanded to graphene domains and were self aligned into graphene arrays. Finally, CH_4 was shut off and furnace was opened up allowing the system to rapidly cool down to room temperature with the flow of H_2 gas. Note that a variety of growth conditions has also been conducted on liquid Cu surface as listed in Table S1 (Supporting Information) to reach the goal of further controllability over graphene growth.

Scanning electron microscopy (SEM) images of the as-grown graphene arrays prepared on liquid Cu surface under 5 sccm (standard cubic centimeters per minute) CH_4 and 300 sccm H_2 for 30 min at 1160 °C at ambient pressure are clearly shown in Figures 1b,c. It is found that the graphene arrays are perfectly spatial self-aligned and well-dispersed in high yield over the whole Cu surface. The arrays alignment with certain preferential orientation with respect to the substrate was also observed and could be related with the crystal structures of Cu. Previous report showed that crystallographic orientation of the copper grains was of fundamental importance in determining the grown graphene.[26] Based on that, it is suggested that the surface of liquid Cu could play a role in the orientation of graphene alignment since different alignment directions at different surface areas are noticed in Figure 1b. The average size of the single hexagonal graphene flake is about 12 μm (Figures 1b–c), defined as the length of the longest diagonals connecting two opposite vertices. The uniformity in graphene size indicates the little deviation in growth rate among the domains under this growth condition. Both the larger and smaller graphene domains were also prepared. Compared to the pre-pattern method to make graphene arrays, liquid Cu surface involves self-movements of uniform graphene flakes on it, allowing for perfect arrangement. During the growth procedure, the appearance of arrays might be related with the formation of thermostable constructures and lead to the force balance over the whole liquid Cu surface. The detailed mechanism would be discussed in the following section. Our method involving liquid phase to fabricate well-aligned graphene arrays provides an alternative to precisely tailor graphene nucleation without complicated processing approaches.

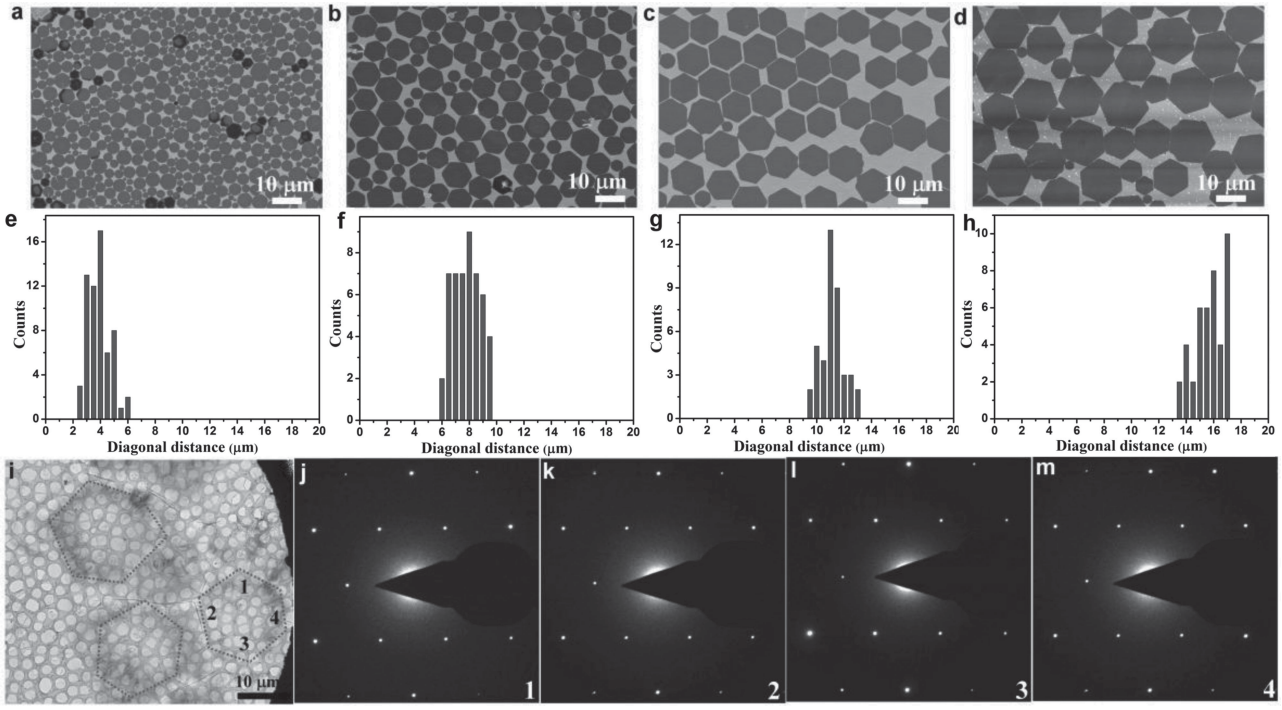

Figure 2. The size evolution of graphene domains under different growth conditions and TEM characterizations of graphene arrays. a–h) SEM images and typical digrams of size distribution of graphene domians while methane flow rate was 12, 8, 5, and 3 sccm, respectively, demonstrating the high controllability over graphene size. Note that the self-aligned graphene arrays at 5 sccm CH_4. i) TEM image showing several hexagonal shaped graphene domains. j–m) Selected area electron diffraction (SEAD) data for small regions indicated 1 to 4. These SAED data confirm the single-crystalline structure of the graphene domains as they have the same set of six-fold symmetric diffraction points.

The characterization of as-grown arrays is crucial to its further applications. Raman spectrum is a non-destructive and powerful technique to identify the number of layers and presence of defects in graphene based on the featured peaks. In our experiments, Raman measurements were performed by using a 514 nm excitation laser on transferred graphene arrays. The transfer procedures are similar to those reported previously.[27] Briefly, the PMMA was spin-coated on the Cu surface and then electrochemical bubbling method was used to isolate the graphene/PMMA film from the Cu surface and finally the PMMA was rinsed by acetone. The optical microscopy of as-transferred graphene arrays (Figure S2a, Supporting Information) clearly shows the obvious contrast, which demonstrates clear transferred graphene arrays on the substrates. The graphene arrays still retain the intrinsic arrangement on arbitrary substrates. Raman spectrum of these graphene arrays transferred onto a 300 nm SiO_2/Si substrate is shown in Figure 1d. The graphene arrays display typical single layer features with two prominent Raman peaks located at 1580 and 2680 cm^{-1}, corresponding to the G and 2D peaks, respectively. The intensity ratio of I_{2D} and I_G is about 3–5 (Figure S2b, Supporting Information). No D peak related to its defect was detected. These results indicate that the as-grown graphene arrays are monolayer and have high quality.

Growth parameters such as carbon source flow rate, growth temperature, and growth time have a large effect on the as-grown graphene. In our experiments, by modulating the flow rate of CH_4, controllable growth of the graphene containing domination of grain size and distribution was successfully achieved. **Figures 2**a–h show graphene grain size and distribution obtained under different growth conditions. The detailed experimental parameters are listed in Table S1 (Supporting Information). When the CH_4 flow rate is kept at 5 sccm for 30 min, the graphene domain is well-distributed and arranged to form perfect arrays. Uniform size of the graphene grains is conducive to the self-alignments to form perfect arrays, while more or less the CH_4 flow rate gives rise to non-uniform graphene grains and thus no ordered graphene arrays were observed. Under the same growth temperature (1160 °C), constant H_2 flow rate and identical growth time, when the CH_4 flow rate decreases from 12, 8, 5 to 3 sccm, the average size of sinlge graphene grain monotonically increases from 3, 8, and 12 to 15 μm as statistically shown in Figures 2e–h. The critical parameters could be related with graphene growth kinetics in which a saturation behavior would happen and thus the grains cease to grow uniformly as size beyond 12 μm.[25] Recently, it was reported that the growth of large-size and single-crystal graphene domain was up to 2.3 mm,[28] however, the required high-demanding growth conditions and complicate processing methods are still met with further limitation in further controllability over graphene growth. Given that the size of graphene domain is an important parameter for graphene growth and applications, growth conditions could be precisely tuned to reach the controllability. Note that graphene nucleation density and growth rate actually influence the final size of graphene domain. For optimized growth conditions in our experiments,

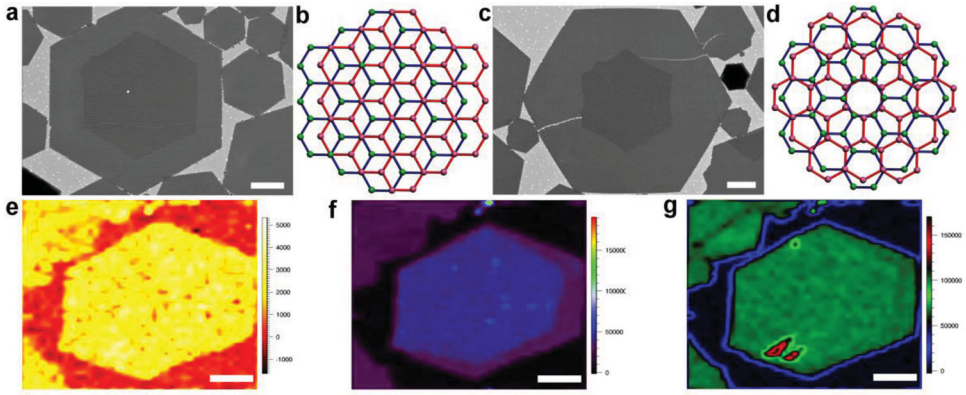

Figure 3. SEM images and Raman mapping of bilayer graphene flakes. a–d) The two orientation of bilayer graphene flakes, aligned, and rotated 30°. The growth condition is 20 sccm CH_4, 300 sccm H_2 for 30 min. e,f) D, G, and 2D peaks mapping of bilayer graphene transferred on Si/SiO_2 substrate. All the scale bars are 10 μm.

large-size graphene domains up to hundreds micrometers or even millimeter scale are easily prepared (Figure S3, Supporting Information). However, the arrangement for large size graphene domains was less controllable and thus the distribution was deviated from arrays. The above phenomena further suggested the optimized and critical growth conditions for graphene arrays. For each as-grown hexagonal graphene grain among the arrays, single crystalline feature was confirmed by transmission electron microscopy (TEM) characterization. Selected area electron diffraction (SAED) patterns together with the images show that six-fold symmetric diffraction points with the same set of patterns were observed over the whole graphene (Figures 2i–m). We tested many individual graphene grains and found that all of them show single crystalline feature from the SAED results. The above data further demonstrate the high quality of the as-grown graphene arrays.

It is reported that bilayer graphene shows great advantage in graphene-based electronics due to its intrinsic opened band gap and thus affording easier functionality designment.[25] In our experiments, increasing methane flow rate directly led in appearance of bilayer graphene on the liquid Cu surface as shown in **Figure 3**. We observed that there existed two kinds of stacked bilayer graphene structures when referring to the orientation of the first and second layer, in which aligned (Figure 3a) and rotated 30° (Figure 3c) with each other. The two corresponding atomic stacked structures are clearly shown in Figure 3b,d, respectively. Statistics shows higher percentage for the aligned orientation, complying to the AB Bernal stacking, which was consistent with previous reports.[25] The appearance of relative orientation of the two layers can be related to the fact that the orientation of second layer is not solely depended on the interaction with the first layer. The Cu can also participate in defining the orientation due to their adhesion. Raman mapping has been conducted to further characterizing the as-grown bilayer graphene (Figure 3e–g). The three characterized peaks of D, G, and 2D clearly showed the uniformity of bilayer graphene, in which the obvious contrast of G peak between the two layers was found. Based on the above data, it is suggested that the liquid Cu method could be advantageous in preparing bilayer graphene due to the high controllability over graphene nucleation.

The introduction of liquid Cu phase during the CVD process allows for some dramatic changes in the graphene growth and arrangement compared to normal solid metal catalyst growth. As the above discussion and previous reports,[18] the liquid phase can confine the nucleation process and eliminate graphene grain boundaries during growth stage, resulting in much larger single-crystal graphene grains with higher quality. The surface tension theory was employed to interpret the graphene arrangement on liquid Cu.[29] As the growth temperature was up to the melting point of Cu, the surface tension of liquid metal could play a critical role in the alignment of graphene domains. The whole liquid Cu surface can be supposed to be a system with certain arc angles in order to keep balance before graphene nuclei were formed. After the first graphene nucleus appeared, its gravity distorts the whole balance of surface tension and thus the system needs additional forces to keep the balance. As the dissociation of carbon atoms proceeds, the second graphene nucleus is formed to fix the balance and then the as-grown two graphene flakes approach as shown in **Figure 4**a. On the liquid Cu surface, the movements of approaching graphene flakes comply to energy-least rule for decreasing surface free energy, the edges of hexagonal graphene flakes with the same energy are parallel arranged together while the vertex with higher energy approaches a vertex of another domain as demonstrated in Figure 4b. For the single hexagonal graphene domain, three directions are employed to arrange two neighboring graphene domains. The detailed edge and vertex arranged modes are displayed in Figure 4c. At the early stage of graphene alignment, we observed that the three hexagonal graphene grains approached (Figure S4, Supporting Information) under the guideline of energy-least principle as mentioned above. During the graphene growth, the same process repeats until the whole liquid Cu surface is covered with graphene, when the system with arranged graphene arrays is still in a balance. We studied the role of time in the whole process (Figure S5, Supporting Information), which clearly showed the evolution and self-alignment of hexagonal graphene grains as time increased. It should be noted that as the growth time further extended, the graphene domains would eventually merge into uniform graphene film as shown in Figure 4d. In our experiments, by modulating flow rate of carbon source,

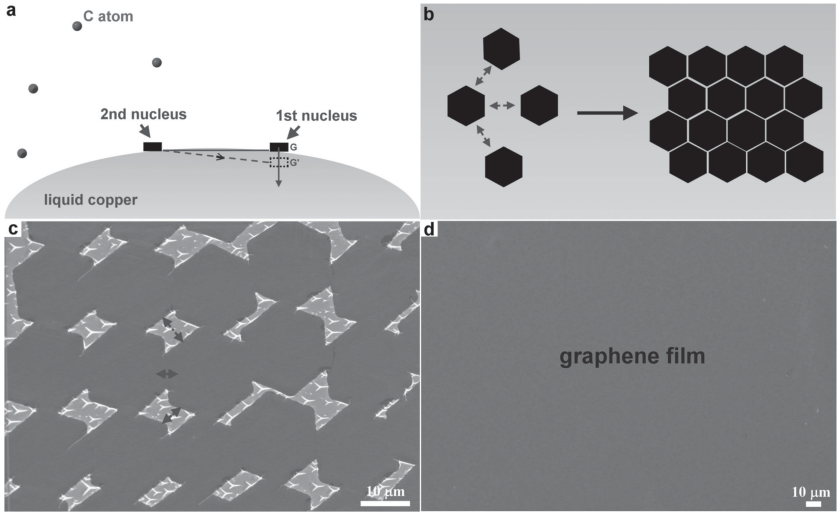

Figure 4. Growth mechanism of self-aligned graphene arrays. a) Scheme of side-view of graphene array growth on liquid Cu surface. b) Scheme of top-view of the edge and point approaching mode of adjacent hexagonal graphene flakes. c) SEM images of as-grown graphene arrays demonstrating the approaching mode between neighboring graphene domains. d) SEM images of large area and uniform graphene film as the arrays further approached.

the nucleation distribution is controlled, thus leads to uniform growth and self-alignment for graphene nuclei. More CH_4 disassociation results in fast graphene growth while less carbon favors slow growth, and both of which lead to obvious size discrepancy among graphene grains and thus not well self-alignment. Control experiments on solid Cu surface have also been conducted. From the SEM images, we could observe that the as-grown graphene grains were dispersed randomly on the solid Cu surface (Figure S6, Supporting Information). The results further illustrated the role of the liquid Cu phase in manipulating the nucleation and dispersion of as-grown graphene grains.

Field-effect transistor (FET) devices were fabricated based on individual single-crystal graphene domain transferred onto 300 nm SiO_2/Si substrates to further characterize the electrical properties of as-grown graphene samples. The measurements were performed at room temperature in air as one device (**Figure 5**). More than 95% of the devices showed linear and

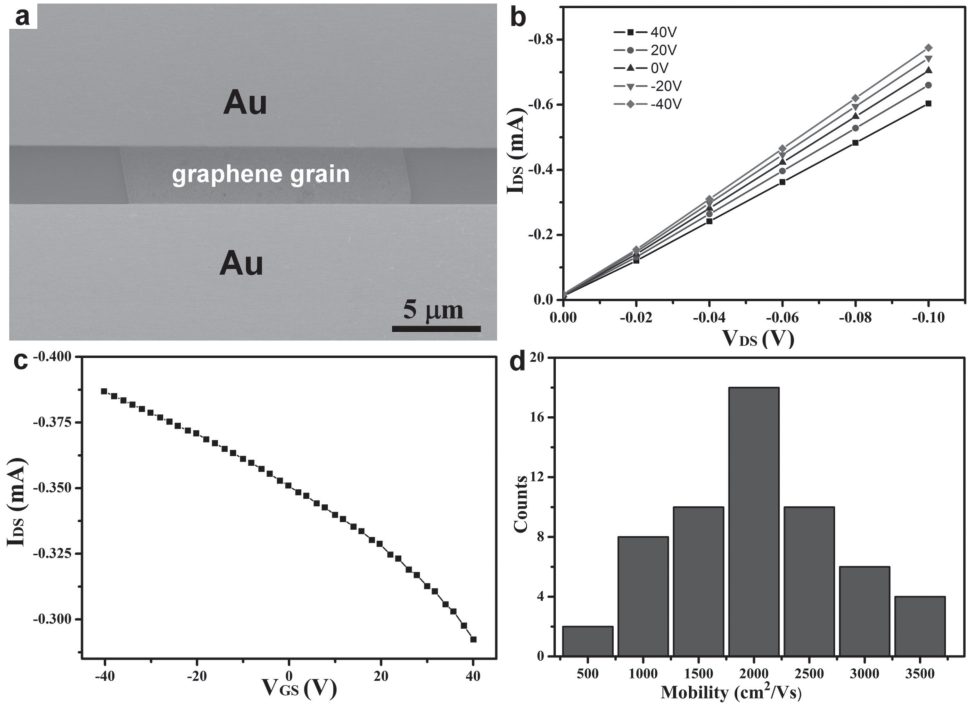

Figure 5. Electrical characteristics of individual single layer hexagonal graphene grain. a) SEM image of the FET device based on an individual graphene grain. b) The output characteristics of the graphene-based FET device. c) The transfer characteristics of the graphene-based FET device. d) Histogram of hole mobility distribution for the 58 devices, ranging from 500 to 3500 $cm^2\ V^{-1}\ s^{-1}$.

reproducible *I–V* curves, demonstrating good ohmic contact between the graphene domains and Au electrodes. The average mobility was calculated to be about 2000 $cm^2 V^{-1} s^{-1}$. 58 devices were constructed and the derived mobilities were found to be ranging from 500 to 3500 $cm^2 V^{-1} s^{-1}$. These values are relatively high compared to those grown on solid copper using the same back-gated FET configuration,[30] reasonably reflecting the good quality of graphene grains. Further improvement on clean transferring technique is a very crucial step for devices fabrication. It is thus important to optimize both the graphene transfer and FET device fabrication processes in order to probe the intrinsic carrier mobility in the future work.

3. Conclusions

We reported the controllable growth of self-aligned hexagonal graphene grains on liquid copper surface at ambient pressure CVD by precisely tuning flow rate of carbon source and other growth parameters. The growth mechanism of graphene arrays on liquid copper surface was firstly probed and the grown graphene arrays show reasonable mobility and high current density, which are comparative with the hexagonal graphene flakes grown on solid Cu. Bilayer graphene was also fabricated, demonstrating high controllability over graphene layer number using liquid Cu approach. The self-aligned graphene arrays should exhibit wide applications in graphene-based electronics for further scale-up production.

4. Experimental Section

50 μm thick Cu foils (99.8% purity) and 100 μm thick W foils (99.95%) were purchased from Alfa Aesar. 2–4 pieces of Cu foils were directly placed on the W foil. Prior to graphene growth, the 1 inch quartz tube was pumped to ≈10 Pa to clean the whole system, and then filled with 200 sccm (standard cubic centimeters per minute) H_2. Subsequently, the quartz tube was heated by furnace (Lindberg/Blue M, TF55035A) to 1160 °C for 40–50 min. Next, annealing treatment was performed in H_2 gas for 20 min. At the graphene growth stage, the H_2 flow rate was changed to the desired value, and CH_4 was then introduced into the chamber. Finally, CH_4 was turned off, and the system was rapidly cooled down to room temperature.

The graphene arrays grown on the Cu surfaces were transferred onto 300 nm SiO_2/Si substrates and TEM grids by the PMMA-assisted electrochemical method.[10,27] The transferred graphene samples were characterized by SEM (Hitachi S-4800, 1 kV), optical microscopy, Raman spectroscopy (Renishaw Invia plus, with laser excitation of 514 nm and spot size of 1–2 μm), and TEM (Tecnai G2 F20 U-TWIN, operated at 200 kV).

The electrical property of individual graphene domain was measured after transferring onto the 300 nm SiO_2/Si substrates. FET devices based on graphene domains were fabricated using our previous method.[31,32] Typically, a 2–5 μm wide nanowire (a rigid "H" type anthracene derivative) was placed onto individual graphene domain, and then a 30 nm gold film was evaporated on the sample. Finally, the organic nanowire was removed by using a micromanipulator, and the desired electrodes were fabricated by mechanically scratching the gold film in order to make isolated FET device. The electrical characteristics of the FET devices were determined by using a Keithley 4200 SCS semiconductor parameter analyzer at room temperature in air. The mobility of charge carriers was extracted from the equation: $\mu_{dev} = \frac{L}{V_D C_{ox} W} \frac{d I_d}{d V_g}$, where L and W are the device channel length and width, respectively, V_D is the voltage between source and drain electrodes, and C_{ox} is the gate capacitance per unit area.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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